## GaN FET Test Kit 2.0



## **Features:**

- GaN Test Kit based on AccoTEST Standard test platform STS8200
- Up to quad site test by one kit, max support 2 test kit with 8 sites test in parallel by the tester
- Fully Floating VI source driven up to 1000V/10A DC
- Low leakage test module included, <1nA Leakage test ability
- Support menu-driven programming
- Support Dynamic Ron Soft Switching Test
- Support soft docking

## Specification (DC):

• Drain to Source

Test Items	Force/Measure Voltage Ranges	Resolution	Accuracy (%FS)	Remark
BVDSS/IDSS	±1000V, ±500V, ±200V, ±100V	16bit	±0.05%	HVI1K
Test_VD_Sweeps_GDS Test_High_ISB Test_VD_GDS_Sub_Id	±1000V, ±500V, ±200V, ±100V	16bit	±0.05%	By HVI1K/FOVI
Test_Vg_ld Test_Vg_ld_lg Test_Vg_ld_Ron	±100V, ±40V, ±20V, ±10V, ±5V, ±2V, ±1V	16bit	±0.05%	By FPVI/FOVI



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**BVDSS/IDSS /VFSD/RDSON** ±100V,±40V, ±20V, 16bit ±0.05% FPVI10\_PLUS Test\_Vg\_Id\_Ron ±10V, ±5V, ±2V, ±1V **Test Items Force Current Ranges** Resolution Accuracy (%FS) Remark VFSD/RDSON FPVI10 PLUS ±10A(Pulsed) 16bit ±0.5% Test\_Vg\_Id\_Ron Low Leakage Measure Resolution Remark **Test Items** Accuracy **Current Ranges** IDSS ±10mA 16bit ±0.1%FS By HVI1K ±1mA 16bit ±(3uA+0.2%) by HV-PAM Test\_VD\_Sweeps\_GDS ±100uA ±(300nA+0.2%) by HV-PAM 16bit Test\_High\_ISB  $\pm 10 \text{uA}$ 16bit ±(50nA+0.5%) by HV-PAM Test\_VD\_GDS\_Sub\_Id ±1uA 16bit ±(10nA+0.5%) by HV-PAM Low VDSon Resolution Accuracy (%FS) Remark **Test Items Measure Ranges** ±100mV 16bit ±1% by QVM RDSON/VDSON ±10mV 16bit ±1% by QVM Test\_Vg\_Id\_Ron ±1mV 16bit ±2% by QVM

#### • Gate to Source

Test Items	Force/Measure Voltage Ranges	Resolution	Accuracy(%FS)	Remark
VTH/IGSSF/ IGSSR/BVGS	±40V, ±20V, ±10V, ±5V, ±2V, ±1V	16bit	±0.05%	By FOVI/FPVI
Test Items	Force /Measure Current Ranges	Resolution	Accuracy(%FS)	Remark
VTH/IGSSF/ IGSSR/BVGSS	±100mA, ±10mA, ±1mA, ±100uA	16bit	±0.1%	By FOVI
	±1A(Pulsed), ±10uA(measure only)	16bit	±0.5%	By FOVI
Test Items	Low Leakage Measure Current Ranges	Resolution	Accuracy(%FS)	Remark
IGSSF/IGSSR/ Test_Vg_lg_Step	±1mA	16bit	±(1.5uA+0.15%)	by LV-PAM
	±100uA	16bit	±(150nA+0.15%)	by LV-PAM
	±10uA	16bit	±(15nA+0.15%)	by LV-PAM
	±1uA	16bit	±(1.5nA+0.15%)	by LV-PAM
	±100nA	16bit	±(0.3nA+0.1%)	by LV-PAM



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## Specification (Dynamic Ron Soft Switching) :

- HV Stress Voltage :  $\leq +1000V$  .
- HV Stress Time : 0~>10S.
- Gate Driver: -30V ~+30V (Windows 30V)
- Toff: <2us
- Tdelay: <10us.
- Id: <10A



